

Please consider the pending claims in light of the references cited in the enclosed Information Disclosure Statement. These references were considered in related U.S. Patent Application Serial No. 09/546,174, filed April 11, 2000, and U.S. Patent Application Serial No. 08/958,460, filed October 28, 1997, now U.S. Patent No. 6,117,345.

William J. Kubida, et al (Customer No. 25235) was appointed the attorney of record in the copending parent case (U.S. Application Serial No. 09/546,174) in a power of attorney filed October 11, 2001 (a copy of which is included herewith). Please confirm that correspondence in this case should be directed to:


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In view of all of the above, claims 21-31 are believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Applicants enclose herewith the fee for filing a continuation application and believe this to be the only fee required for this amendment and response. Should any additional fees be required, please charge Deposit Account 50-1123.

Respectfully submitted,

November 20, 2001

  
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CLEAN VERSION OF THE AMENDMENT

IN THE SPECIFICATION

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The present application is a continuation of copending U.S. Patent Application Serial No. 09/546,174, filed April 11, 2000, which is a continuation of U.S. Patent Application Serial No. 08/958,460, filed October 28, 1997, now U.S. Patent No. 6,117,345, which claimed priority from U.S. Provisional Patent Application Serial No. 60/041,790, filed April 2, 1997, all the disclosures of which are herein specifically incorporated by this reference.

IN THE CLAIMS

21. (New) A method for forming conducting structures separated by gaps on a substrate, comprising the steps of:  
providing a substrate and a wiring layer above the substrate;  
forming a cap layer above the wiring line layer;  
forming a mask layer above the cap layer;  
etching the mask layer to expose selected portions of the cap layer;  
etching the cap layer, and the wiring line layer, at the locations where the cap layer is exposed by the etched mask layer, to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material within the gaps at a sputtering rate sufficient to fill the gaps, using high density plasma chemical vapor deposition.

22. (New) The method of claim 21, wherein the cap layer comprises a material selected from the group consisting of a silicon nitride material and an oxynitride material.

23. (New) The method of claim 21, wherein a remaining portion of the cap layer on at least one wiring line has a rectangular shape in cross section.

24. (New) The method of claim 21, wherein a remaining portion of the cap layer on at least one wiring line has a trapezoidal shape in cross section.

25. (New) The method of claim 24, wherein the trapezoidal shape includes top and bottom surfaces parallel to one another and side surfaces that extend inwardly from the bottom surface to the top surface.

26. (New) The method of claim 21, wherein the remaining portion of the cap layer on at least one wiring line has a triangular shape in cross section.

27. (New) The method of claim 21, wherein a remaining portion of the cap layer on at least one wiring line has, in cross section, a rectangular shape having its upper corners etched away.

28. (New) The method of claim 21, wherein a remaining portion of the cap layer is partially etched and redeposited into the gaps during the high density plasma chemical vapor deposition process.

29. (New) The method of claim 21, wherein a remaining portion of the cap layer is partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

30. (New) The method of claim 21, wherein the mask layer is a patterned photoresist layer.

31. (New) The method of claim 21, further comprising the formation of a surface layer between the substrate and the wiring line layer, the surface layer being a barrier between the substrate and wiring line layer.

IN THE SPECIFICATION

[This application claims priority from provisional application Serial No. 60/041,790, filed April 2, 1997.] The present application is a continuation of copending U.S. Patent Application Serial No. 09/546,174, filed April 11, 2000, which is a continuation of U.S. Patent Application Serial No. 08/958,460, filed October 28, 1997, now U.S. Patent No. 6,117,345, which claimed priority from U.S. Provisional Patent Application Serial No. 60/041,790, filed April 2, 1997, all the disclosures of which are herein specifically incorporated by this reference.